DEVICE ISOLATION FOR SEMICONDUCTOR DEVICES

ABSTRACT

Exemplary embodiments of the present invention disclose a semiconductor assembly having at least one isolation structure formed. The semiconductor assembly comprises: a first trench in a semiconductive substrate; a second trench extending the overall trench depth in the semiconductive substrate by being aligned to the first trench; and a planarized insulation material substantially filling the first and second trenches. The isolation structure separates a non-continuous surface of a conductive region. General process steps to form the isolation structure comprise: forming a mask over a semiconductor substrate assembly; forming a first trench into the semiconductor substrate assembly using the mask as an etching guide; forming an insulation layer on the surface of the first trench; forming a semiconductive spacer on the side wall of the first trench; forming a second trench into the semiconductor substrate assembly at the bottom of the first trench by using the semiconductive spacer as an etching guide; forming an isolation filler in the first and second trenches, the isolation filler substantially consuming the semiconductive spacer and thereby substantially filling the first and second trenches; and planarizing the isolation filler.